REMARKS

This is in response to the Office Action of November 14, 2003. Claims 1-24 were rejected. Claims 1-3, 5-7, 10-13, 15-22, and 24 were amended. Claims 4 and 14 were canceled. Claims 1-3, 5-13, and 15-24 are pending.

Claims 1-10, 16, and 20 were rejected under 35 U.S.C. § 112. Claim 1 was amended to eliminate the language that the Examiner found confusing with the change being supported by original claim 11 and paragraph [1116] of Applicant's specification.

Claims 6 and 16 were amended to recite "a MIPS32™ or MIPS64™ architecture." While the Examiner requested that these terms be spelled out, Applicant notes that this would be inappropriate because MIPS32™ and MIPS64™ are trademarked names of specific architectures, not acronyms. Support for this amendment is found in paragraph [1135] of Applicant's specification.

Claims 10 and 20 were amended to include definitions found in Table 7 and as further described on pages 30 to 34. Applicant also wishes to thank the Examiner for identifying a typographical error in these claims. Paragraph [1119] of Applicant's specification clearly indicates that the logical OR operation is used to link several of the operations. Two parentheses were also missing from the equation in claims 10 and 20. Applicant has corrected claims 10 and 20 in accordance with the equation in paragraph [1119] of Applicant's specification.

Claims 1, 4-6, 8, 11, 14-16, and 18 were rejected under 35 U.S.C. 102(b) as being anticipated by Moughani et al. (U.S. Pat. No. 5,970,246). Claims 2, 3, 12, and 13 were rejected under 35 U.S.C. 103(a) as being obvious over Moughani in view of Alpert (U.S. Pat. No. 5,621,886). Claims 7, 9, 17, and 19 were rejected under 35 U.S.C. 103(a) as being obvious over Moughani in view of Moyer (U.S. Pat. 5,812,868). Claims 22 and 23 were rejected under 35 U.S.C. 103(a) as being obvious over Moughani.

Applicant has amended independent claims 1, 11, 21, 22, and 24 to include additional limitations not taught or suggested by the cited references. The independent claims were amended to clarify that a tracing control can be defined for each of a

plurality of operating states of a processor and that each operating state has an associated control input that determines whether tracing is enabled for the operating state. Support for this amendment is found, for example, on paragraph [1116] of Applicant's specification. Applicant has also amended the independent claims to include a limitation comparable to claim 4 that the operating states comprise a plurality of processor modes. The dependent claims were amended to be in accordance with the changes to the independent claims.

One benefit of Applicant's claimed invention is that tracing is automatically adjusted when the processor transitions from one operating state to another operating state. Control of tracing is based upon both the current operating state and upon a control input for the current operating state. This permits, for example, a debug operation to trigger or inhibit tracing based upon the entry or exit from one or more operating states, such as different processor modes, increasing the flexibility with which designing a debugging mechanism, as described in paragraph [1116] of Applicant's specification.

Another benefit of applicant's claimed invention of claims 7, 10, 17, and 20 is that tracing is automatically adjusted depending upon both the processor mode and the particular process that the processor is running. As described in paragraph [1117] of Applicant's specification, tracing can be triggered based upon the identification of a particular process. For example, in a multi-tasking system, each task or process has an ASID value that can be used in the debugging process to identify particular processes that need to be debugged.

Applicant respectfully submits that the cited prior art does not teach or suggest the above-described limitations. Moughani is directed towards the problem of permitting tracing of operational code in a data processing system while maintaining the access protection of specific memory areas, as described in column 1, lines 46-50 and column 2, lines 7-10 of Moughani. In the supervisor mode, a supervisor sets a trace bit in an access protect unit 20 to define memory access privileges in the user mode. See, e.g., column 2, lines 50-62 and column 3, line 51 to column 4, line 4. In the user mode, if a user accesses an address in a memory segment, a trace bit in the access protect unit is checked to

determine if tracing of access protected memory segment is allowed, as described in column 4, lines 41-46.

Note that Moughani teaches controlling tracing in only one mode, the user mode. For example, there is no provision for control inputs to control tracing when the processor is in supervisor mode. Additionally, there is no teaching or suggestion for controlling tracing depending upon the particular process that the processor is running in a particular processor mode.

In regards to independent claims 1, 11, 21, 22, and 24, the Examiner cited only the Moughani reference. Moughani does not teach or suggest a system having a plurality of operating states in which for each operating state a predefined tracing control is based on a current operating state and upon a control input for the particular operating state.

In regards to dependent claims 7, 10, 17, and 20, Moughani does not teach or suggest effecting a predefined trace control based upon a processor mode, an identity of a process being run on a processor, and control inputs for each processor mode and an identity of a process being run.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is now in condition for allowance. The Examiner is invited to contact the undersigned if there are any residual issues that can be resolved through a telephone call.

The Commissioner is hereby authorized to charge any appropriate fees to Deposit Account No. 03-3117.

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